

Technical Description

The Equipment Under Test (EUT) is a Azzaro Wanted By Night Headphones 2021 with Bluetooth audio playback feature, which occupies a frequency range of 2402MHz to 2480MHz. The EUT supports Bluetooth 3.0 and BLE. The EUT is powered by 3.7V internal rechargeable battery (3.7VDC)

2.4GHz Bluetooth:

Modulation Type: GFSK

Antenna Type: Integral, Internal (PCB Trace)

Antenna gain is 0dBi

Frequency Range: 2402MHz - 2480MHz

Conducted RF Power range is -4dBm to 4dBm

The main components are described below:

1. U1 AC6956A is the 2.4GHz Bluetooth RF radio core
2. Y1 24MHz crystal is operating clock for U1

AC6956A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 1.1

Date: 2019.12.27

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

AC6956A Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 240MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codecs supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 30-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, SNR >= 95dB
- Three channels 16-bit ADC , SNR >= 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- three channels Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.1+BR+EDR+BLE specification
- Meet class1 class2 and class3 transmitting

power requirement

- Support GFSK and $\pi/4$ DQPSK all paket types
- Provides +6dbm transmitting power
- receiver with -90dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdpl2cap profile

Peripherals

- One full speed USB 2.0 OTG controller
- Four multi-function 16-bit timers, support capture and PWM mode
- Three 16-bit PWM generator for motor driving
- Three full-duplex basic UART, UART0 and UART1 supports DMA mode
- Two SPI interface supports host and device mode
- One hardware IIC interface supports host and device mode
- Built-in Cap Sense Key controller
- 9 channels 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO for internal digital and analog circuit supply
- 1uA current consumption in the soft-off mode
- Built-in LDO for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 5.5V
- VDDIO is 2.2V to 3.6V
- RTCVDD is 2.2V to 3.6V

Packages

- QFN32(4mm*4mm)

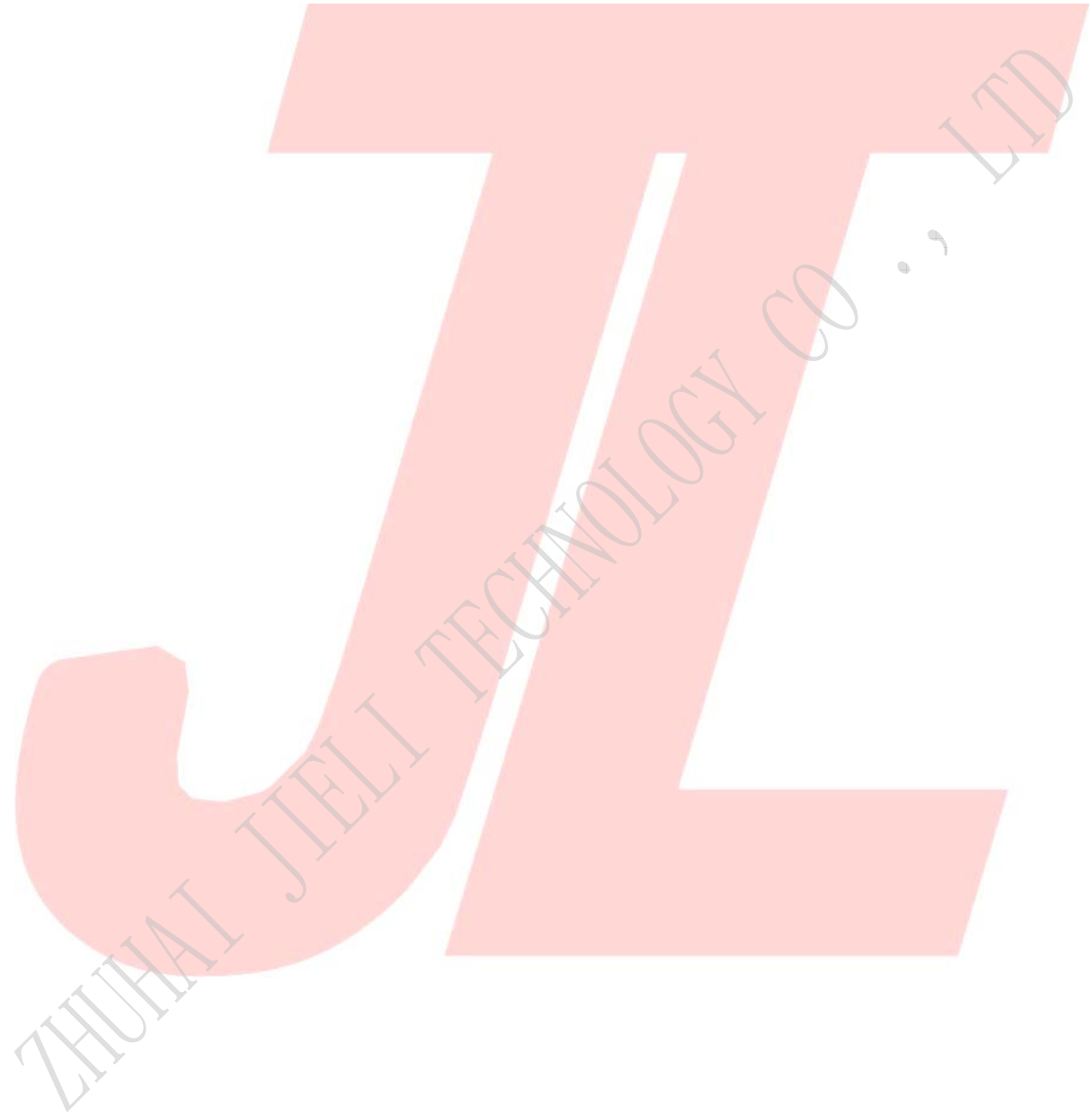
Temperature

- Operating temperature: -20°C to +70°C

- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Stereo headset
- Bluetooth Mono headset
- Bluetooth TWS headset



Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

1、 Pin Definition

1.1 Pin Assignment

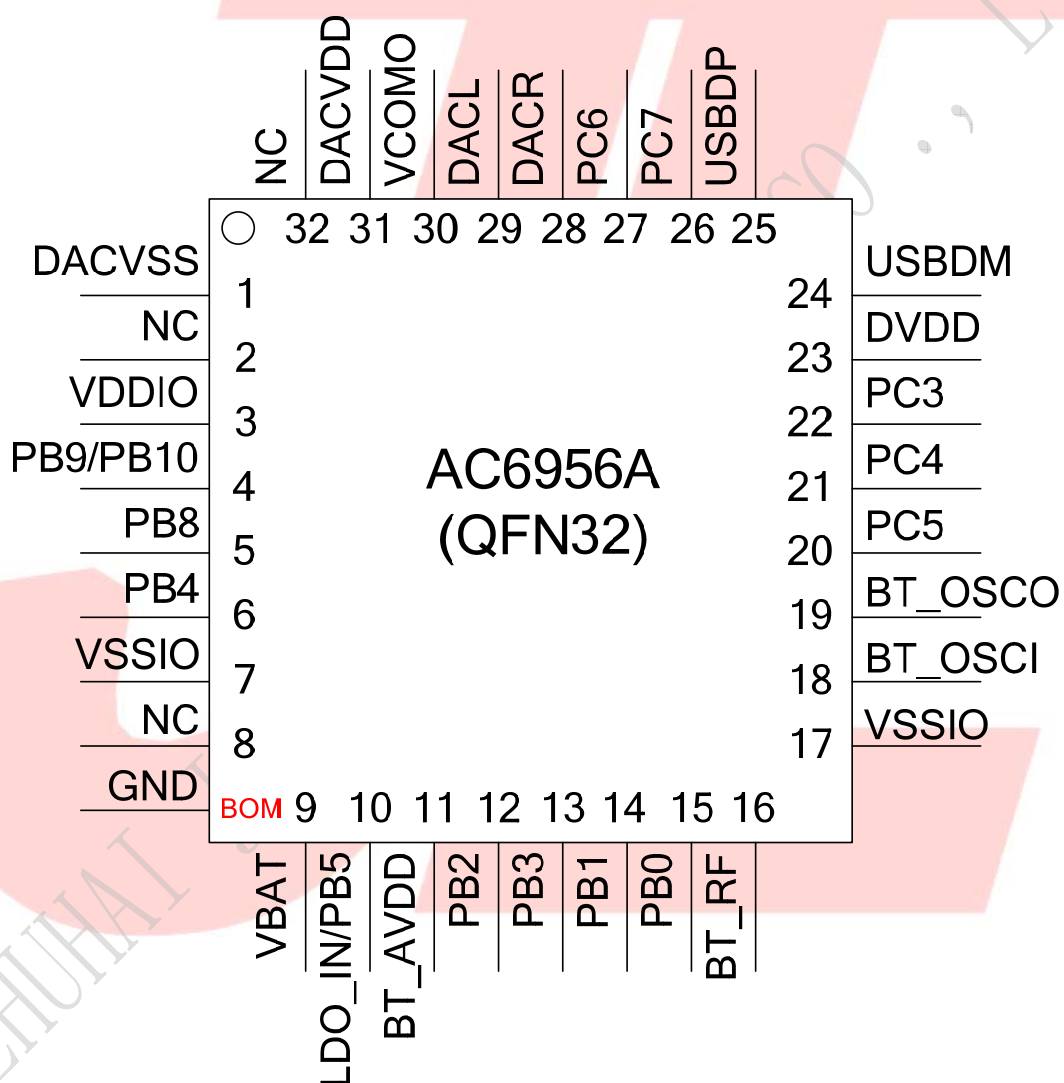


Figure 1-1 AC6956A_QFN32_4x4 Package Diagram

1.2 Pin Description

Table 1-1 AC6956A_QFN32_4x4 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	DACVSS	P	/	Ground	
2	NC				
3	VDDIO	P	/	IO Power 3.3v	
4	PB10	I/O	24/8	GPIO	AMUX2R: Analog Channel2 Right; SPI2DOA: SPI2 Data Out(A); ADC9: ADC Input Channel 9; UART2RXC: Uart2 Data In(C); PWMCH3L: Motor PWM Channel3(L);
	PB9	I/O	24/8	GPIO	AMUX2L: Analog Channel2 Left; SPI2CLKA: SPI2 Clk(A); CAP0: Timer0 Capture; UART2TXC: Uart2 Data Out(C); PWMCH3H: Motor PWM Channel3(H);
5	PB8	I/O	24/8	GPIO	AMUX1R: Analog Channel1 Right; SPI2_DIA: SPI2 Data In(A); ADC8: ADC Input Channel 8; CLKOUT1: Clk Out1;
6	PB4	I/O	24/8	GPIO	IIC_SCL_C: IIC SCL(C); ADC7: ADC Input Channel 7; UART0TXB: Uart0 Data Out(B); LVD: Low Voltage Detect Input; PWMCH2H: Motor PWM Channel2 (H);
7	VSSIO	P	/	Ground	
8	NC				
9	VBAT	P	/	LDO Power	
10	LDO_IN	P	/	Charge Power 5v	
	PB5	I/O	8	GPIO (High Voltage Resistance)	PWM3: Timer3 PWM Output; CAP1: Timer1 Capture; UART0TXC: Uart0 Data Out(C); UART0RXC: Uart0 Data In(C);
11	BT_AVDD	P	/	BT Power 1.3v	
12	PB2	I/O	8	GPIO	SPI1DIA: SPI1 Data In(A);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

				(High Voltage Resistance)	PWMCH1L: Motor PWM Channel1 (L);
13	PB3	I/O	24/8	GPIO	PWM2: Timer2 PWM Output; ADC6: ADC Input Channel 6;
14	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset; SPI1DOA: SPI1 Data Out(A); ADC5: ADC Input Channel 5; TMR2: Timer2 Clock Input; UART1RXA: Uart1 Data In(A);
15	PB0	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKA: SPI1 Clock(A); UART1TXA: Uart1 Data Out(A); PWMCH1H: Motor PWM Channel1(H);
16	BT_RF	/	/		
17	VSSIO	P	/	Ground	
18	BT_OSCI	I	/	OSC In	
19	BT_OSCO	O	/	OSC Out	
20	PC5	I/O	24/8	GPIO	SD1CLKA: SD1 Clock(A); SPI1DOB: SPI1 Data Out(B); UART2RXD: Uart2 Data In(D); IIC_SDA_B: IIC SDA(B); ADC13: ADC Input Channel 13; PWMCH5L: Motor PWM Channel5(L);
21	PC4	I/O	24/8	GPIO	SD1CMDA: SD1 Command(A); SPI1CLKB: SPI1 Clock(B); UART2TXD: Uart2 Data Out(D); IIC_SCL_B: IIC SCL(B); ADC10: ADC Input Channel 10; PWMCH5H: Motor PWM Channel5(H);
22	PC3	I/O	24/8	GPIO	SD1DAT0A: SD1 Data0(A); SPI1DIB: SPI1 Data In(B);
23	DVDD	P	/	Core Power	
24	USBDM	I/O	4	USB Negative Data (pull down)	UART1RXD: Uart1 Data In(D); IIC_SDA_A: IIC SDA(A);
25	USBDP	I/O	4	USB Positive Data (pull down)	UART1TXD: Uart1 Data Out(D); IIC_SCL_A: IIC SCL(A); ADC12: ADC Input Channel 12;
26	PC7	I/O	/	GPIO	MIC_BIAS: Microphone Bias Output
27	PC6	I/O	24/8	GPIO	MIC: MIC Input Channel; ADC11: ADC Input Channel 11;

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

28	DACR	O	/		DAC Right Channel
29	DACL	O	/		DAC Left Channel
30	VCOMO	/	/		DAC Reference Output
31	DACVDD	P	/		Power supply for audioDAC logic
32	NC				

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-20	+70	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	2.2	5.5	V
LDO_IN	Charger Voltage	4.5	5.5	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	VDDIO+0.3	V

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	
LDO_IN	Charger Voltage	4.5	5.0	5.5	V	
V _{3.3}	Voltage output	—	3.3	—	V	VBAT = 5V, 100mA loading
V _{BT_AVDD}	Voltage output	—	1.3	—	V	VBAT=5V, 100mA loading
V _{DACVDD}	DAC Voltage	—	2.7	—	V	VBAT = 5V, 10mA loading
I _{L3.3}	Loading current	—	—	150	mA	VBAT = 5V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	—
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	—
I _{Charge}	Charge Current	20		320	mA	Charge current at fast charge mode
I _{Trinkl}	Trickle Charge Current	20	45	70	mA	V _{BAT} <V _{Trinkl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	—	$0.3 \cdot V_{DDIO}$	V	$V_{DDIO} = 3.3V$
V_{IH}	High-Level Input Voltage	$0.7 \cdot V_{DDIO}$	—	$V_{DDIO} + 0.3$	V	$V_{DDIO} = 3.3V$
IO output characteristics						
V_{OL}	Low-Level Output Voltage	—	—	0.33	V	$V_{DDIO} = 3.3V$
V_{OH}	High-Level Output Voltage	2.7	—	—	V	$V_{DDIO} = 3.3V$

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PB0~PB10 PC6	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
PC7			10K	10K	
PB5			10K	10K	
USBDP	4mA	—	1.5K	15K	
USBDM	4mA		180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	—	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	—	-75	—	dB	
S/N	—	95	—	dB	
Crosstalk	—	-80	—	dB	
Output Swing		1		Vrms	1KHz/-60dB 10Kohm loading With A-Weighted Filter
Dynamic Range		90		dB	
DAC Output Power	11		—	mW	32ohm loading

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	1KHz/-60dB
S/N	—	90	91	dB	1KHz/-60dB
THD+N	—	-70	—	dB	
Crosstalk	—	-80	—	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		4	6	dBm	25°C, Power Supply VBAT=5V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1		dB	25°C, Power Supply VBAT=5V 2441MHz
$\pi/4$ DQPSK	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.8.2 Receiver

Basic Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 QFN32_4x4

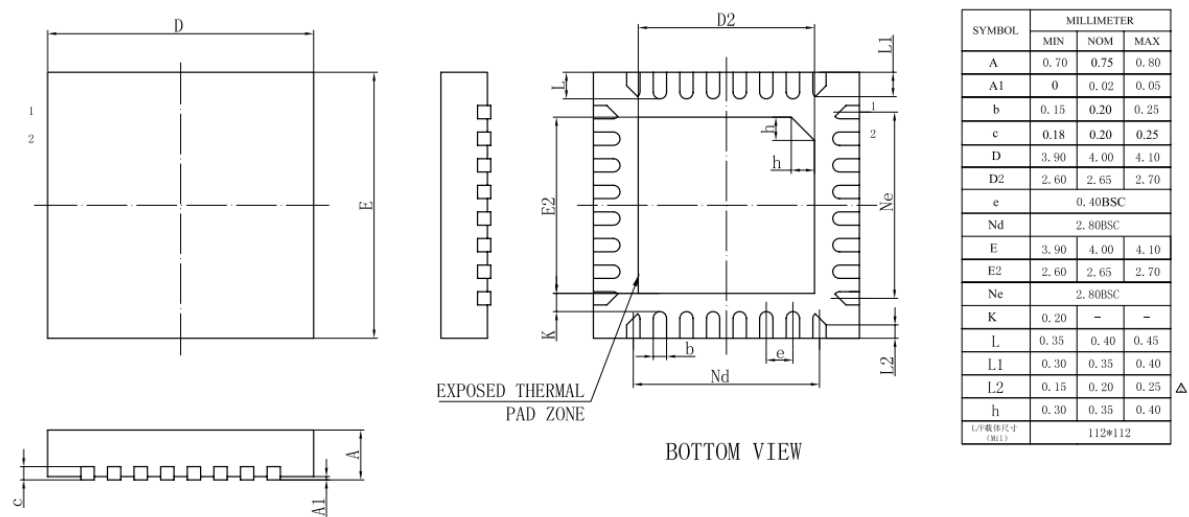


Figure 3-1 AC6956A_QFN32_4x4 Package

4、Revision History

Date	Revision	Description
2019.12.25	V1.0	Initial Release
2019.12.27	V1.1	Delete PB7, Updata Featrues

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.